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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,867	02/19/2004	Kazuya Hizawa	OKI.390C	1983

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EXAMINER	
NOVACEK, CHRISTY L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 11/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/780,867	HIZAWA, KAZUYA	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-10 and 21-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-10 and 21-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/283,189.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/2/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed August 29, 2005.

Drawings

The replacement drawings were received on August 29, 2005. These drawings are approved. The objections to the drawings stated in the previous office action are withdrawn.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 3-10 and 21-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itonaga (US 20020061639, previously cited) in view of Yu et al. (US 20030029715, previously cited).

Regarding claim 21, Itonaga discloses preparing a substrate (1) having a silicon region (7), forming a metallic layer (8) of a first thickness on the silicon region by a sputtering method, forming a protective layer (9) on the metallic layer such that the protective layer has a second thickness that is greater than the first thickness, forming a metallic silicide layer (10a/10b/10c) in an interface between the silicon region and the metallic layer under the protective layer by a first heat treatment, such that the metallic silicide layer has a high resistance crystalline structure, removing the protective layer, and subjecting the metallic silicide layer to a second heat treatment after removing the protective layer so that the metallic silicide layer has a low resistance crystalline structure (para. 0066-0138). Because the protective layer of Itonaga is made of the same material (titanium-nitride) and because it is made to be thicker than the

metallic layer, it appears that the protective layer of Itonaga inherently possesses the function of protecting the metallic layer from a surrounding atmosphere. See *In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 229 (CCPA 1971) "where the Patent Office has reason to believe that a functional limitation asserted to be critical for establishing novelty in the claimed subject matter may, in fact, be an inherent characteristic of the prior art, it possesses the authority to require the applicant to prove that the subject matter shown to be in the prior art does not possess the characteristics relied on "); and *In re Fitzgerald*, 619 F.2d 67, 205 USPQ 594 (CCPA 1980) (a case indicating that the burden of proof can be shifted to the applicant to show that the subject matter of the prior art does not possess the characteristic relied on whether the rejection is based on inherency under 35 U.S.C. 102 or obviousness under 35 U.S.C. 103).

Further regarding claim 21, although Itonaga discloses sputtering the metallic layer onto the substrate, Itonaga does not disclose any particular sputtering method. Like Itonaga, Yu discloses a process for sputtering a refractory metal layer onto the source/drain regions of a silicon substrate and heat-treating the metal layer to react with the silicon substrate to form a metal silicide layer (para. 0093-0094). Yu discloses a silicide-forming process that advantageously reduces process complexity, while improving processing efficiency and throughput (para. 0011). The process taught by Yu involves the steps of heating the substrate at a predetermined temperature, forming the metallic layer on the silicon region of the heated substrate by a straight sputtering method so as to sputter straightly to the silicon region, and forming a metallic silicide layer in an interface between the silicon region and the metallic layer by a heat treatment (para. 0066-0080). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the sputtering process taught by Yu to form the metallic

layer of Itonaga because Itonaga discloses using a sputtering process to form the layer and because Yu teaches that his sputtering process advantageously reduces process complexity, while improving processing efficiency and throughput.

Regarding claims 3, 25 and 31, Yu discloses that the predetermined temperature can be in the range of 10°C-500°C (para. 0068).

Regarding claim 4, Yu discloses that the metallic layer can be formed by a long-throw or collimate sputtering method (para. 0028, 0031, 0032, 0035, 0041, 0042, 0058).

Regarding claims 5, 24, 26 and 32, Itonaga discloses that the metallic layer can be cobalt or titanium (para. 0138).

Regarding claim 6, Itonaga discloses that the depth of the silicon region is larger than the first thickness of the metallic layer (Fig. 1B).

Regarding claim 7, Itonaga discloses that the protective layer can be made of titanium-nitride (para. 0069).

Regarding claim 8, Itonaga discloses that the first thickness of the metallic layer is 8nm (para. 0069).

Regarding claim 9, Itonaga fails to disclose that the second thickness of the protective layer is equal to or more than 30nm. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use routine experimentation to determine an appropriate thickness of which to form the protective layer of Itonaga, depending upon the materials being used for the metallic layer and the protection layer and the atmospheric conditions of the deposition and annealing processes, because such variables of art recognized importance are subject to routine experimentation and discovery of an optimum value for such variables is

obvious. See *In re Aller*, 105 USPQ 233 (CCPA 1955). Furthermore, Applicant's specification contains no disclosure of either the critical nature of the claimed dimension or any unexpected results arising therefrom.

Regarding claim 10, Itonaga discloses a source region and a drain region (7) of a MOS transistor are formed in the silicon region wherein the metallic silicide layer is formed (para. 0066).

Regarding claim 22, Itonaga discloses that the MOS transistor includes a polysilicon gate (4), forming a metallic layer on the gate, and forming the metallic silicide layer in an interface between the gate and the metallic layer (Fig. 1C; para. 0066).

Regarding claim 23, Itonaga discloses preparing a substrate (1) having a silicon region (7), forming a metallic layer (8) of a first thickness on the silicon region by a sputtering method, forming a protective layer (9) on the metallic layer, forming a first metallic silicide layer (10a/10b/10c) under the protective layer by a first heat treatment, such that the metallic silicide layer has a high resistance crystalline structure, removing the protective layer, and subjecting the metallic silicide layer to a second heat treatment after removing the protective layer so that the metallic silicide layer has a low resistance crystalline structure (para. 0066-0138). Although Itonaga discloses sputtering the metallic layer onto the substrate, Itonaga does not disclose any particular sputtering method. Like Itonaga, Yu discloses a process for sputtering a refractory metal layer onto the source/drain regions of a silicon substrate and heat-treating the metal layer to react with the silicon substrate to form a metal silicide layer (para. 0093-0094). Yu discloses a silicide-forming process that advantageously reduces process complexity, while improving processing efficiency and throughput (para. 0011). The process taught by Yu involves the steps

of heating the substrate at a predetermined temperature, forming the metallic layer on the silicon region of the heated substrate by a straight sputtering method so as to sputter straightly to the silicon region, and forming a metallic silicide layer in an interface between the silicon region and the metallic layer by a heat treatment (para. 0066-0080). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the sputtering process taught by Yu to form the metallic layer of Itonaga because Itonaga discloses using a sputtering process to form the layer and because Yu teaches that his sputtering process advantageously reduces process complexity, while improving processing efficiency and throughput.

Regarding claims 27 and 33, Itonaga discloses that the first metallic silicide layer is a metal-rich silicide (Ti_2Si) and the second metallic silicide layer is a stoichiometric metal silicide layer ($TiSi_2$) (para. 0071, 0076).

Regarding claims 28 and 34, Applicant's specification discloses that the orientation of the metallic layer is a result of the temperature at which the layer is sputtered onto the substrate (Fig. 12). Applicant's specification discloses that at sputtering temperatures of 400°C, the metallic layer will be most likely to have an orientation of a (200) surface (Fig. 12). Yu discloses that the metallic layer is sputtered onto the substrate at a temperature of 10-500°C. Therefore, it appears that the metallic layer of Itonaga, deposited as taught by Yu, would inherently possess the function of having a (200) surface orientation. See *In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 229 (CCPA 1971) "where the Patent Office has reason to believe that a functional limitation asserted to be critical for establishing novelty in the claimed subject matter may, in fact, be an inherent characteristic of the prior art, it possesses the authority to require the applicant to prove that the subject matter shown to be in the prior art does not

possess the characteristics relied on "); and *In re Fitzgerald*, 619 F.2d 67, 205 USPQ 594 (CCPA 1980) (a case indicating that the burden of proof can be shifted to the applicant to show that the subject matter of the prior art does not possess the characteristic relied on whether the rejection is based on inherency under 35 U.S.C. 102 or obviousness under 35 U.S.C. 103).

Regarding claims 29 and 35, Itonaga discloses that the temperature of the first heat treatment is lower than the temperature of the second heat treatment (para. 0071, 0076).

Regarding claim 30, Itonaga discloses preparing a substrate (1) having a silicon region (7), forming a metallic layer (8) of a first thickness on the silicon region by a sputtering method, forming a protective layer (9) on the metallic layer, forming a first metallic silicide layer (10a/10b/10c) under the protective layer by a first heat treatment, such that the metallic silicide layer has a high resistance crystalline structure, removing the protective layer, and subjecting the metallic silicide layer to a second heat treatment after removing the protective layer so that the metallic silicide layer has a low resistance crystalline structure (para. 0066-0138). Although Itonaga discloses sputtering the metallic layer onto the substrate, Itonaga does not disclose any particular sputtering method. Like Itonaga, Yu discloses a process for sputtering a refractory metal layer onto the source/drain regions of a silicon substrate and heat-treating the metal layer to react with the silicon substrate to form a metal silicide layer (para. 0093-0094). Yu discloses a silicide-forming process that advantageously reduces process complexity, while improving processing efficiency and throughput (para. 0011). The process taught by Yu involves the steps of heating the substrate at a predetermined temperature, forming the metallic layer on the silicon region of the heated substrate by a straight sputtering method so as to sputter straightly to the silicon region, and forming a metallic silicide layer in an interface between the silicon region and

the metallic layer by a heat treatment (para. 0066-0080). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the sputtering process taught by Yu to form the metallic layer of Itonaga because Itonaga discloses using a sputtering process to form the layer and because Yu teaches that his sputtering process advantageously reduces process complexity, while improving processing efficiency and throughput.

Response to Arguments

Applicant's arguments filed August 29, 2005 have been fully considered but they are not persuasive.

Regarding the rejection of claim 21 as being unpatentable over Itonaga in view of Yu, Applicant argues that the rejection is allegedly improper because Itonaga teaches forming an amorphous layer as an intermediate step. However, whether or not Itonaga teaches forming an amorphous layer as an intermediate step is irrelevant in so far as there is no language in Applicant's claims that precludes an amorphous layer from being formed as an intermediate step.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
November 1, 2005

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Approved CK 11/1/05

REPLACEMENT SHEET

F-00ED0748

FIG.1

PRIOR ART

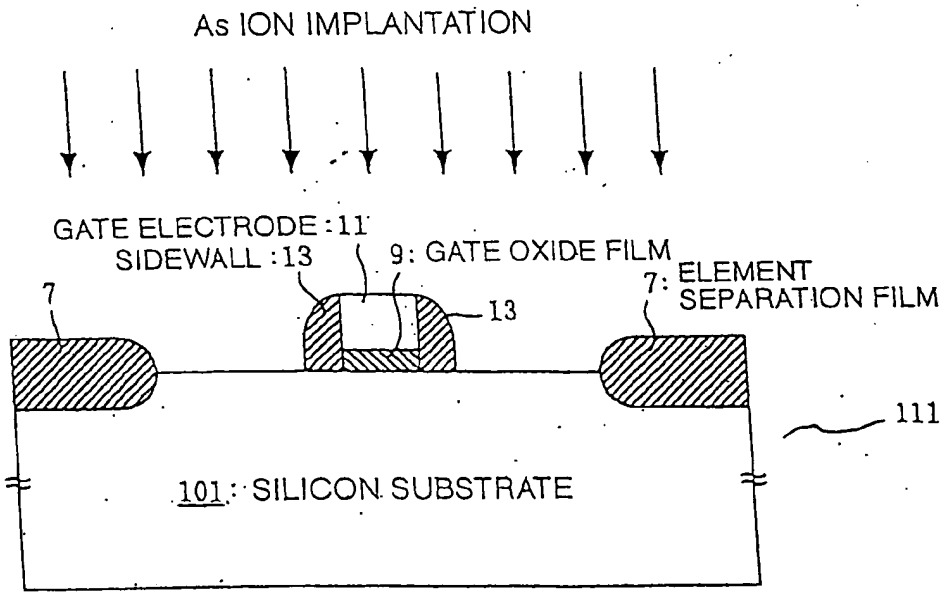

FIG.2

PRIOR ART